Reducing Extrinsic Performance-Limiting Factors in Graphene Grown by Chemical Vapor Deposition

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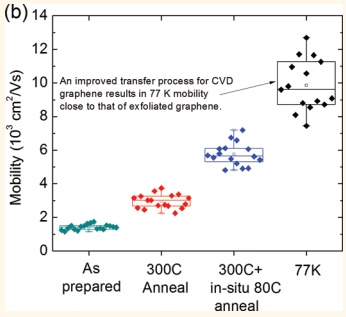
ABSTRACT Field-effect transistors fabricated on graphene grown by chemical vapor deposition (CVD) often exhibit large hysteresis accompanied by low mobility, high positive backgate voltage corresponding to the minimum conductivity point (V_{min}), and high intrinsic carrier concentration (n_0). In this report, we show that the mobility reported to date for CVD graphene devices on SiO_2 is limited by trapped water between the graphene and SiO_2 substrate, impurities introduced during the transfer process and adsorbates acquired from the ambient. We systematically study the origin of the scattering impurities and report on a process which achieves the highest mobility (μ) reported to date on large-area devices for CVD graphene on SiO_2: maximum mobility (μ_{max}) of 7800 $cm^2/(V \cdot s)$ measured at room temperature and 12 700 $cm^2/(V \cdot s)$ at 77 K. These mobility values are close to those reported for exfoliated graphene on SiO_2 and can be obtained through the careful control of device fabrication steps including minimizing resist residue and non-aqueous transfer combined with annealing. It is also observed that CVD graphene is prone to adsorption of atmospheric species, and annealing at elevated temperature in vacuum helps remove these species.



KEYWORDS: graphene · transistor · chemical vapor deposition · mobility · scattering

Graphene grown by chemical vapor deposition (CVD) on Cu provides a promising pathway for the fabrication of graphene field-effect transistors (FETs) on a large scale.[1] However, the performance of CVD graphene FETs reported to date is degraded relative to FETs fabricated using exfoliated graphene. CVD graphene FETs often exhibit strong hysteresis accompanied with low mobility, large V_{min}, and high n_0. It has been reported that the presence of water molecules at the graphene/SiO_2 interface enhances molecular adsorption from ambient resulting in p-doping, gate hysteresis, and degraded mobility in exfoliated graphene.[2−9] Although Gannett *et al.* recently reported that high mobility (as high as 37 000 $cm^2/(V \cdot s)$) can be achieved when CVD graphene is transferred to a hexagonal boron nitride (h-BN) substrate,[10] the technique is not currently scalable because large-area h-BN films are not yet available. However, this does not rule out extrinsic factors such as water and adsorbates affecting FET performance when h-BN is integrated with graphene, as well. It has been reported that mobility as high as 200 000 $cm^2/(V \cdot s)$ at an electron density of 2×10^{11} cm^{-2} at 5 K can be achieved by suspending annealed (400 K) exfoliated graphene *in vacuo*.[11] It has also been reported that high mobility with significantly reduced gate hysteresis can be achieved on exfoliated graphene when the SiO_2 is coated with a layer of hydrophobic hexamethyldisilazane (HMDS).[12] We have also transferred CVD graphene onto a SiO_2 substrate coated with HMDS and observed a room temperature mobility of ~6000 $cm^2/(V \cdot s)$ (data not shown), where the graphene was transferred in water and was measured *in vacuo* after an 80 °C *in situ* anneal. However, coating the SiO_2 with a layer of HMDS is not desirable for the realization of large-scale graphene electronic devices.[3] On the other hand, it has been reported that defects can be reduced by exfoliating graphene in a nitrogen-rich environment.[13] The literature also provides examples describing various annealing treatments anticipated to remove spurious surface contaminants from graphene, but a systematic study of the details with a statistically significant data set has not been performed and is required to advance the state-of-the-art. We find that optimization of the transfer process is critical for achieving

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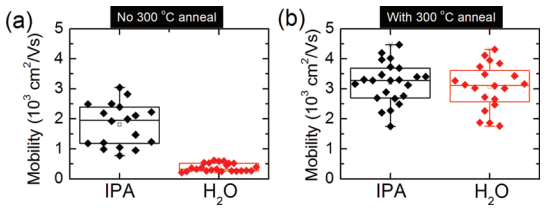

Figure 1. FET mobility of CVD graphene measured in vacuum for (a) graphene transferred in IPA and in water for 18 and 23 devices, respectively; (b) same devices annealed at 300 °C for 3 h.

high-quality CVD graphene FETs. In this study, we report on the influence of the graphene transfer medium (aqueous *vs* non-aqueous medium) and of the post device fabrication annealing on graphene FETs' performance.

RESULTS AND DISCUSSION

Consistent with very recent reports on individual devices fabricated on exfoliated graphene,[14] we find that the process detail for graphene transfer from the Cu substrate to a dielectric surface such as SiO_2/Si is a critical step in achieving high-quality FETs. We have modified the graphene transfer process from using water as the last step to using isopropyl alcohol (IPA) and also performed anneals at 300 °C under ultrahigh vacuum (UHV) conditions. We find that the IPA minimizes water trapped between the graphene and the SiO_2 substrate, and that the anneal further removes residual interfacial water and poly(methyl methacrylate) (PMMA).[15]

Figure 1a shows two sets of FETs transferred to SiO_2 in IPA and water. In order to eliminate run-to-run variations, the graphene used in this experiment was grown during the same CVD growth run, that is, on the same piece of Cu foil, and transferred on two SiO_2/Si substrates that were cleaved from the same silicon wafer prior to the transfer of graphene. The as-prepared devices of the graphene transferred in water show an average mobility (μ_{avg}) of ~380 ± 130 cm^2/(V·s), while the average mobility of those transferred in IPA is ~1810 ± 710 cm^2/(V·s), almost a factor of 5 times higher. We attribute this enhancement in mobility to reduced interfacial water molecules trapped during the transfer process. The two samples were then removed from the vacuum probe station and annealed *ex situ* at 300 °C under UHV in another chamber for 3 h.[15] After the 300 °C anneal, the samples were moved back to the vacuum probe station within ~10 min of the annealing process; thus the samples were exposed to the laboratory ambient during the 10 min. Figure 1b shows the mobility of the same set of devices after the 300 °C UHV anneal. The average mobility for the IPA transferred samples increased to 3200 ± 670 from 1810 ± 710 cm^2/(V·s), whereas the devices fabricated on graphene using the water transfer process increased to 3060 ± 750 from ~380 ± 130 cm^2/(V·s). The mobility of both sets of postannealed devices is well within the experimental variation of the mobility and uncertainty of the measurement. The improvement for both cases is significant and suggests that, even in the case of the IPA transfer, there could be volatile residual species, such as hydroxyls from water, under the graphene that is removed by the 300 °C UHV anneal. Therefore, we conclude that the 300 °C anneal under UHV improves the graphene mobility by (i) removing interfacial water molecules or their derivatives and (ii) removing PMMA residue from the surface of the graphene. It is also noted that the annealing appears to result in a smoother surface as seen by atomic force microscopy analysis in air.[15]

Figure 2a shows the measured device resistance (R_{total}) *versus* backgate−source voltage (V_{GS}) curves of a representative device out of about 15 FETs on the same sample with graphene transferred to SiO_2 using the IPA process, following a series of annealing and PMMA treatment conditions. After the first transport measurement on the as-prepared devices, the sample was taken out of the probe station, PMMA was respun onto the sample, and then the PMMA was stripped off using acetone as described above. The sample was immediately transferred back to the vacuum probe station after the acetone strip and pumped for 15 h (~10^{-6} mbar). The extracted mobility was found to be ~2060 cm^2/(V·s): higher than the original as-prepared value. The same sample was then *ex situ* reannealed at 300 °C under UHV, and the average mobility was again found to increase to 2410 from 2060 cm^2/(V·s) but not higher than the first anneal, suggesting that graphene might have been damaged during the second PMMA process. X-ray photoelectron spectroscopy (XPS) analysis (see ref 15) shows the presence of PMMA residue after the graphene is transferred onto SiO_2 and that it is drastically reduced after the 300 °C UHV anneal. Since the mobility shows an increase after the 300 °C UHV anneal and the XPS data show removal of the PMMA after annealing, we attribute the residue of PMMA to play a significant role in reducing mobility. However, the observed difference between the PMMA respun (step iii) and the as-prepared (step i) measurements also suggests that the removal of PMMA is not the only mechanism contributing to the improved mobility.

The contact resistance (R_c) values for these devices were typically observed to lie in the 500−750 Ω range (saturated resistance values in Figure 1a). The anneal was not seen to considerably affect the measured R_c. This is attributed to the fact that the anneal was performed on finished devices. The graphene in the contact region is therefore protected by the metal and is not substantially affected by the anneal.

In order to further improve the properties of the graphene FETs transferred in IPA, we also performed an *in situ* 80 °C anneal in the vacuum-cryostat probe station after the 300 °C UHV *ex situ* anneal. The *in situ* 80 °C anneal temperature was limited by the vacuum-cryostat probe station heating capability. A set of 18 FETs were

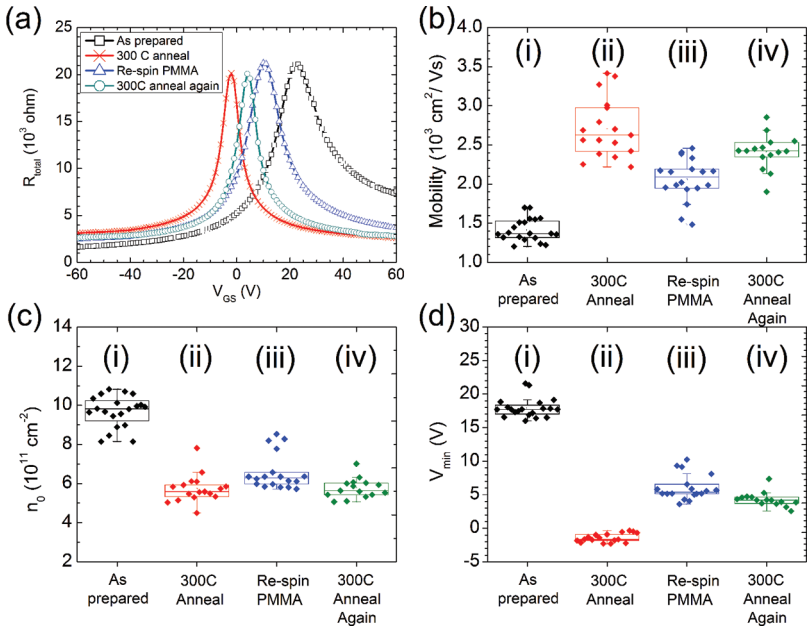

Figure 2. (a) $R_{total}-V_{GS}$ of a representative device measured after exposure to 15 h of vacuum at room temperature in the following cycle: (i) as-prepared, (ii) after a 300 °C UHV anneal for 3 h, (iii) respinning PMMA followed by acetone strip-off, and (iv) anneal again at 300 °C in UHV for 3 h. (b) Mobility, (c) impurity concentration, and (d) gate voltage corresponding to the minimum conductance are extracted for the device preparation conditions in (a).

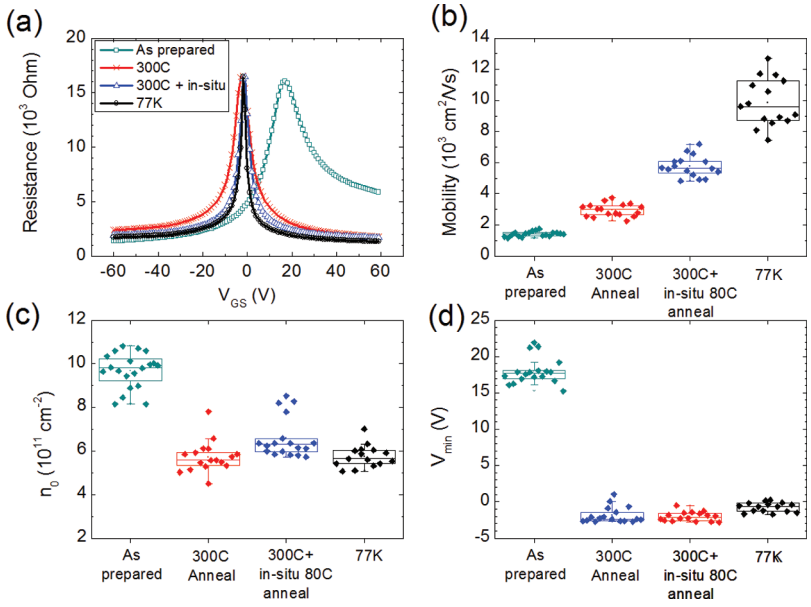

Figure 3. (a) $R_{total}-V_{GS}$ for the as-prepared devices, annealed at 300 °C in UHV, annealed at 300 °C in UHV, plus *in situ* annealed at 80 °C and measured at room temperature, compared to the same device measured at 77 K after 300 °C UHV anneal followed by an 80 °C *in situ* anneal; (b) mobility, (c) impurity concentration, and (d) V_{min} of 18 as-prepared graphene FETs after the conditions described in (a).

measured in the as-prepared state after 15 h of vacuum pumping in the probe station. Then the samples were removed and annealed *ex situ* at 300 °C in UHV (and thus exposed to the air), followed by an *in situ* anneal in the probe station at 80 °C under vacuum for 15 h. Figure 3 shows a summary of the data where the overall trend presented in Figure 1 is reproduced and also shows that the mobility is further improved after the *in situ* 80 °C vacuum anneal for 15 h, as shown in Figure 3b. The increase in mobility is attributed to the reduction of residual adsorbates by the *in situ* 80 °C vacuum anneal.

The sequence of anneals, in an attempt to create a clean graphene film, clearly increases the mobility from ~1420 to an average of 5760 ± 680 $cm^2/(V\cdot s)$, as a result of decreasing the impurity concentration, n_0, and shifting the V_{min} toward that of intrinsic graphene. A maximum extracted mobility of 7200 $cm^2/(V\cdot s)$ at room temperature is obtained which exceeds typical

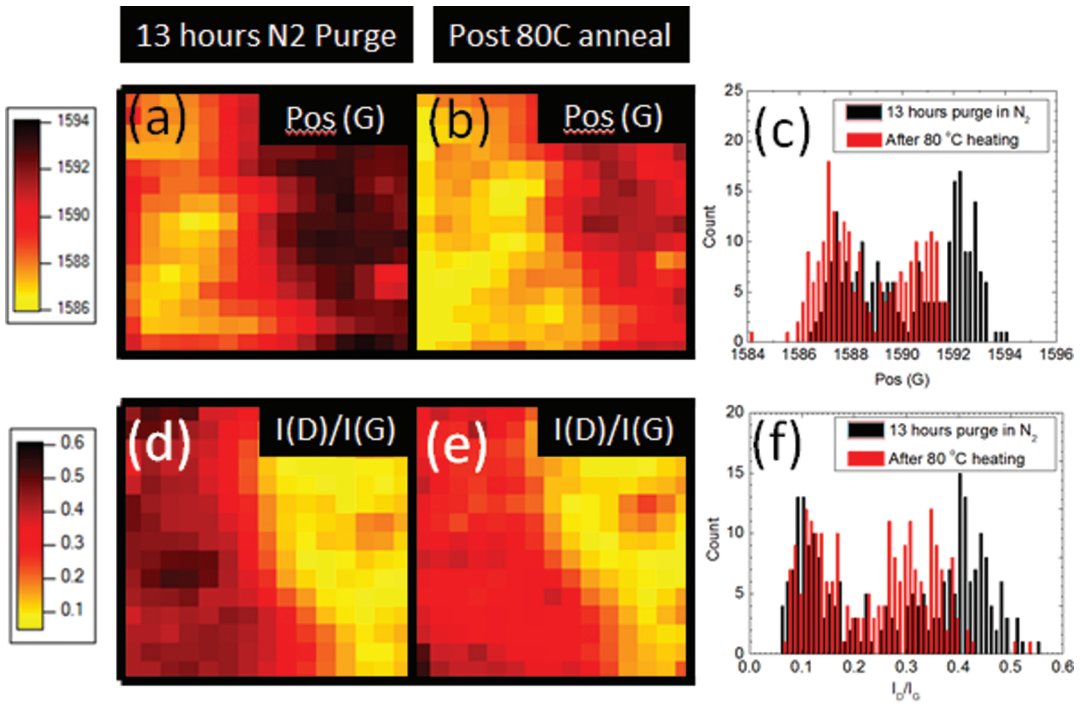

Figure 4. Raman maps of G-band position (Pos(G)) measured in (a) N_2 environment before and (b) after an 80 °C *in situ* anneal. (c) Pos(G) histogram is red-shifted, indicating a reduction in p-type doping. Raman maps of I_D/I_G after (d) N_2 purging and (e) 80 °C *in situ* anneal, showing I_D/I_G is reduced after the 80 °C anneal. (f) Reduction effect is more significant in the more defective regions of the CVD graphene, as noted in the corresponding histogram.

reports of mobility for CVD graphene on *large devices*, 65 μm × 15 μm, to date. Fringing fields have been shown to result in the overestimation of measured mobility in smaller graphene devices; therefore, larger devices were used in this study to avoid this effect.[16]

We speculate that the mechanism for mobility improvement by the 80 °C *in situ* anneal is due to additional desorption of residual contaminants. Since the sample had been previously annealed at 300 °C (under UHV) resulting in substantial contaminant removal, the adsorbates removed during this 80 °C *in situ* anneal were likely acquired during the 10 min atmospheric exposure period from the movement of the devices from the UHV anneal chamber to the vacuum probe station and are not easily removed by the probe station vacuum exposure only at room temperature. We have previously shown that defects in CVD graphene as measured by the Raman D-band preside primarily at the grain boundaries with very few defects within the domains.[17] Furthermore, the average mobility of CVD graphene with a non-optimized transfer process and measured in air increases with increasing domain size. The sensitivity of CVD graphene to ambient exposure may be related to the domain boundary defects. Further work is required to understand the reactivity of grain boundaries and its impact on transport properties. We also note that devices on exfoliated graphene are much smaller than the device size used to evaluate the CVD graphene in this paper, which can lead to substantial errors in mobility extraction.[16]

Figure 4 shows a comparison of room temperature Raman spectra of graphene after (i) 13 h of purging in a N_2 environmental cell and then (ii) after an 80 °C *in situ* anneal under flowing N_2 in the cell. The graphene sample was transferred using IPA and then annealed at 300 °C under UHV before transferring to the Raman environmental cell. Figure 4a shows the Raman map of the G-band Raman shift ("Pos(G)") before the *in situ* anneal. The map shows a variation in the G-band frequency which can be associated with an inhomogeneous doping level across the graphene film. Figure 4b further shows the map of the "G"-band position (Pos(G)) after the *in situ* anneal where p-type doping is reduced, as indicated by the lower G-band wavenumber.[18] Figure 4c shows the histogram of the Pos(G) distribution where the average Pos(G) Raman shifts are 1591.0 and 1588.7 cm^{-1} before and after anneal, respectively. The Pos(G) is red-shifted, indicating the removal of acceptor dopants during the *in situ* annealing process.[18] Figure 4d–f shows that the ratio of D-band to G-band intensity (I_D/I_G) is reduced after the 80 °C *in situ* anneal. Since the reduction is apparent over the entire mapped area, the reduction does not appear to be localized—that is, on grain boundaries, wrinkles, and perhaps adlayers (small regions of bilayer graphene)—but instead is nearly uniform across the graphene basal plane. It is not conclusively understood why the D-band intensity reduces after the *in situ* anneal, although possibilities may include (i) healing or passivation of defective sites and/or (ii) removal of amorphous

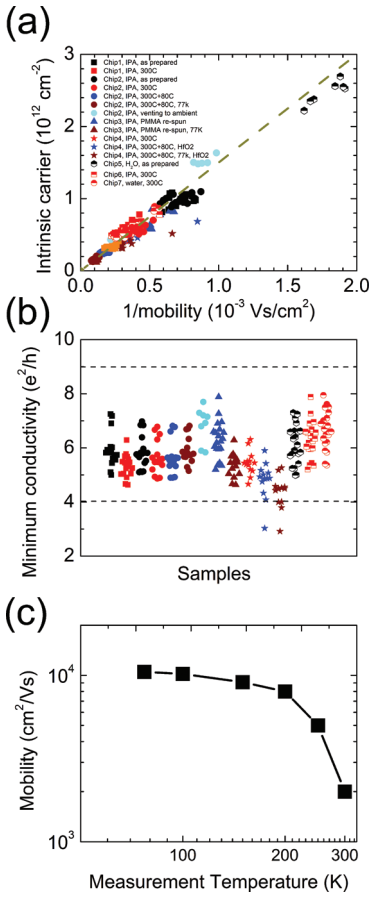

Figure 5. (a) Intrinsic carrier density *vs* inverse mobility and (b) minimum conductivity extracted for a large number of devices with different interfacial conditions (IPA or water), anneal history (300 °C UHV/80 °C *in situ* and combinations thereof), presence of capping HfO_2, and measurement temperature (room temperature/77 K). (c) Mobility as a function of temperature.

carbon[19] upon heating in an inert environment. Further research is required to understand the reduction of I_D/I_G upon the *in situ* anneal. The reduction in I_D/I_G is likely correlated with reduced scattering centers and hence leads to the improved mobility shown in Figure 3.

Finally, Figure 5a shows a plot of the impurity-induced carrier density *versus* inverse mobility for a number of devices with different interfacial conditions (IPA or water), anneal history (300 °C UHV/80 °C *in situ*), with/without a HfO_2 top dielectric,[20] and measurement temperature (room temperature *vs* 77 K). It is found that the product of mobility and impurity density is a constant, with $\mu \cdot n_0 \approx 1.15 \times 10^{15}/(V \cdot s)$. Comparing this with the value $\mu \cdot n_{imp} \approx 1.5 \times 10^{15}/(V \cdot s)$ predicted by Adam *et al.* yields $n_0 \approx 0.23 n_{imp}$, which agrees well with exfoliated graphene, $n_0/n_{imp} \approx 0.2-0.5$ on SiO_2.[21,22] Figure 5b shows the corresponding minimum conductivity with most devices having a value between 4 and 8 e^2/h. This linear relation and reasonable minimum conductivity values, which hold over a wide range of mobility values, indicates that, despite the presence of grain boundaries, ad-layer regions, and wrinkles, the electrical properties of CVD graphene are still surprisingly similar to that of ideal exfoliated graphene from natural graphite. *The widely reported low CVD graphene mobilities in the literature are thus largely due to extrinsic causes associated with processing.*

To further study the mobility scattering mechanism, we performed low temperature, 77 K, transport measurements. The data in Figure 3 show that, as the temperature is decreased to 77 K, the mobility increased to $\mu_{avg} = 9860 \pm 1530$ cm^2/(V·s) and $\mu_{max} = 12700$ cm^2/(V·s). The temperature dependence of the mobility for one of the devices is shown in Figure 5c. Chen *et al.* reported that the large temperature dependence of mobility at temperatures above ~200 K is limited by the substrate phonon scattering.[23] The temperature-independent behavior for temperatures below ~200 K is limited by scattering from defects or impurities present in SiO_2. The 77 K mobility of our CVD graphene on SiO_2 after the 300 °C UHV and 80 °C *in situ* anneal is similar to that of exfoliated graphene on SiO_2 (for example, as reported in ref 23). This suggests that the amount of impurity scattering for our CVD graphene after annealing is similar to that of exfoliated graphene on SiO_2. The precise conditions of the transfer process and anneals necessary to achieve these results may vary depending upon the CVD graphene growth conditions. Our work suggests that surface preparation and cleaning of the graphene is critical in achieving high-mobility CVD graphene devices. Given the effect of adsorbates, PMMA residue, and trapped water, it is likely that these process improvements can be applied to other substrates, such as h-BN, to improve the overall electrical performance of graphene devices.

CONCLUSIONS

In summary, we have obtained transferred CVD graphene with extracted mobilities comparable to that of exfoliated graphene on SiO_2. The treatments reported in this paper, including the replacement of the graphene transfer medium from water to IPA, the 300 °C UHV anneal, and the *in situ* 80 °C vacuum anneal, all serve as methods to reduce *extrinsic* impurities or defects that degrade the graphene electrical performance.

METHODS

CVD graphene was synthesized on copper foils using CH_4 and H_2 environment for a period of 3 min at $T > 1000$ °C; the CVD process details are described elsewhere.[1,15] The graphene/Cu stack was spin-coated with PMMA, and the Cu was then etched away in a 0.5 M ammonium persulfate for 12 h.

The graphene/PMMA stack is then placed in either deionized water or IPA before transferring to a SiO_2/Si substrate wafer (p-doped, 90 nm thermal SiO_2) and blow-dried with dry N_2. The PMMA/graphene/SiO_2/Si stack was then heated on a hot plate in air at 220 °C for 5 min to cure the PMMA. This temperature is selected as it is slightly higher than the PMMA glass transition temperature (T_g < 165 °C), which allows the PMMA to reflow as it is annealed. This process has been found to result in more uniform transferred graphene layers with minimum cracking of the graphene.[24] After the sample is cooled to room temperature, the PMMA was stripped by soaking in acetone for 2 h at room temperature before device fabrication. XPS of this surface shows that some PMMA residue remains after the strip,[15] and that longer IPA soaks, even at elevated temperatures, do not reduce the residue below detectable limits. The graphene channel was then defined by photolithography and an O_2 plasma etch followed by source/drain contact formation using Ni/Au (40 nm/30 nm) deposited by e-beam evaporation.

For this study, a constant device size, length of 65 μm and width of 15 μm, was used to study the effects of the transfer process and annealing on the transport characteristics. The device size selection was based on prior work by Venugopal *et al.* showing that the device dimensions, the SiO_2 thickness, and the constant mobility model provide mobilities consistent with the Drude and Hall measurement methods at high fields and reproduce mobility values in the literature.[16] The gate dependence of channel resistance is measured at a constant drain source bias (V_{DS} = 20 mV). The electrical transport parameters, including μ, V_{min}, and n_0 are extracted using the constant mobility model described by Kim *et al.*[25] We have previously shown that this technique provides mobility values consistent with other methods (*e.g.*, Hall).[16]

All electrical data reported here are measured in a vacuum-cryostat probe station at room temperature, after 15 h of vacuum exposure ($\sim 10^{-6}$ mbar), unless otherwise specified. The mobility values reported here represent the average of electron and hole mobilities, extracted from several (≥15) devices. An *ex situ* annealing process at 300 °C for 3 h in UHV ($\sim 10^{-9}$ mbar) to remove PMMA residue utilized herein is described in detail elsewhere.[15] It is noted that the stated anneals are performed on fully fabricated backgate FET devices. The Raman spectral maps were acquired using a Nicolet Almega XR spectrometer with a 532 nm laser excitation source over a 40 × 40 μm^2 area with a 1 μm step size; Raman measurements were also performed using an environmental cell to control the sample ambient.

Conflict of Interest: The authors declare no competing financial interest.

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